Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N/C**
2. **INPUT A**
3. **GND**
4. **INPUT B**
5. **OUT B**
6. **VDD**
7. **OUT A**
8. **N/C**

**.080”**

**4 2**

**3 3**

**5 6 7**

**.060”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential:**

**Mask Ref: CLM4426/27/28**

**APPROVED BY: DK DIE SIZE .060” X .080” DATE: 8/15/19**

**MFG: CALOGIC THICKNESS .011” P/N: AS4426**

**DG 10.1.2**

#### Rev B, 7/1